Amendments to the Specification

Please amend the first paragraph on Page 8 as follows:

The process of the present invention begins, as in the prior art, with the formation of an opening such as a hole or trench (such as 15 in FIG. 1) in the surface of an integrated circuit. Most commonly, said surface will be that of a dielectric layer, but that is not a requirement of the invention. The hole extends from an upper surface of the dielectric layer to a first wiring layer. Typically the trench width used will be between about 0.1 and 15 microns, the hole diameter between about 0.1 and 0.5 microns, and the depth of the opening will be between about 0.4 and 1 microns. The trench is formed by patterning and etching the dielectric layer. The trench comprises a bottom surface, a mouth, and side walls. In addition, the trench is disposed to fully overlap the hole and to extend a depth below the upper surface of the dielectric layer. The depth of the trench is greater than a depth of the hole, which extends a distance from the bottom surface of the trench to the first wiring layer.

Please amend the second paragraph on Page 8 as follows:

Next, if a copper damascene process is being used, a barrier layer of a material such as tantalum, tantalum nitride, titanium nitride, or tungsten nitride is laid down to a thickness between about 100 and 500 Angstroms. Whether or not a barrier layer is used, a seed layer of metal (specifically copper if a damascene process is being used) is next laid down to cover the inside surfaces of the trench or hole. In addition to copper, the metal may be gold or silver. The thickness of this seed layer is between about 800 and 2,500 Angstroms and it is deposited by means of a PVD (sputtering or vacuum evaporation).